REMARKS

Claim 20 has been added. Support for this claim may be found in the specification on at least page 4, line 23 through page 5, line 19, as well as in Figures 1 and 2. Claims 1 – 20 are present in the subject application. Claim 11 has been amended to correct minor typographical errors. Claims 1 – 10 have been withdrawn per the restriction requirement of June 16, 2005. Applicants retain the right to file a divisional on the withdrawn claims. In addition, should the pending product claims be allowed, the examiner is requested to consider whether rejoinder of the withdrawn method claims is appropriate per MPEP § 806.05(f).

In the Office Action dated August 26, 2005, the Examiner rejected claims 11 – 19 under 35 U.S.C. §102(e). Favorable reconsideration of the subject application is respectfully requested in view of the following remarks.

Claims 11 – 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,806,557 to Ding. The Examiner takes the position that the Ding patent discloses all the features recited within these claims. This rejection is respectfully traversed since the Ding patent does not disclose, teach, or suggest the features recited in independent claim 11 of a conductive layer that surrounds an electrical component, wherein the conductive layer bonds the encasing layer to the substrate.

Ding discloses a hermetically sealed microdevice 20 including a device microstructure 22, a substrate 24, and a silicon cap 30. *See* col. 4, ll 22 – 26 and Figures 1A and 1B. The cap is bonded directly to the substrate by a non-adhesive hermetic seal. Specifically, the substrate is

connected to the cap using either an anodic bonding process or a frit glass bonding process. *See* col. 4, lines 40 – 45 and 57 – 60. The microdevice may further include conductive traces 27 extending through the sides of the cap and into the cavity 38 formed by the cap. *See* col. 5, ll 45 – 47 and FIG. 1B.

The Office action equates the conductive traces of the Ding patent with the conductive bonding layer of the instant invention. The conductive traces of Ding, however, are not the equivalent of the bonding layer recited in claim 11 because the trace does not secure the cap to the substrate. The specification, on page 5, lines 6 – 10, explains the metal bonding layer transports bonding current during anodic bonding. The bonding frames patterned in the metal bonding layer, in turn, bond a glass wafer to the substrate, creating a sealed cavity encasing one or more electronic components. In contrast, the substrate of the Ding patent is *directly secured* to the cap by anodic or glass frit bonding processes. Even when the conductive traces are present, Ding explains that a frit glass bond is preferably used *to attach the cap to the substrate*. *See* col. 5, lines 50 – 54. That is, when the traces are present, the cap is still directly bonded to the substrate. Each conductive trace simply passes through one portion of the rim of the cap and, as such, do not create a bonding surface for the cap. Since the trace does not secure the cap to the substrate, no conductive bonding layer is present in the structure as required in claim 11.

In addition, claim 11 of the instant invention requires the conductive bond layer to *surround* the electronic device. As explained in the specification, the conductive bond frame 107 surrounds the system to be packaged, with the system being positioned *inside* the bond frame.

Consequently, the electrical component is encircled by the electrically conductive bond layer. *See* page 5, line 5 through page 6, line 2; page 6, lines 11 – 12; and Figures 2 and 3. In contrast, the conductive traces of Ding do not surround the microdevice. Instead, the traces pass through opposite sides of the cap rim to connect the microdevice 22 (located within the cavity 38) to wires or chips outside of the cavity. *See* col. 5, lines 45 – 60 and Figure 1B. That is, each trace extends from a position outside the cap, through a portion of the cap rim, and to a position inside the cap (i.e., into the cavity). As such, neither trace *surrounds* the electronic component as required by independent Claim 11.

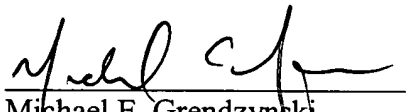
Since the Ding patent does not disclose, teach, or suggest the features recited within independent claim 11 as discussed above, this claim is considered to be in condition for allowance. Claims 12 – 19 depend, either directly or indirectly, from independent claim 1 and, therefore, include all the limitations of their parent claim. These dependent claims are considered to be in condition for allowance for substantially the same reasons discussed above in relation to their parent claim and for further limitations recited in the claims.

New claim 20 includes features similar to those of independent claim 11. As discussed above, the Ding reference does not disclose, teach, or suggest an electrically conductive layer surrounding an electronic component, wherein the electrically conductive layer is configured to bond the encasing layer to the substrate.

In view of the foregoing, Applicants respectfully request the Examiner to find the application to be in condition for allowance with claims 11 – 20. However, if for any reason the

Examiner feels that the application is not now in condition for allowance, he is respectfully requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

Respectfully submitted,



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Hand Delivered on: November 28, 2005